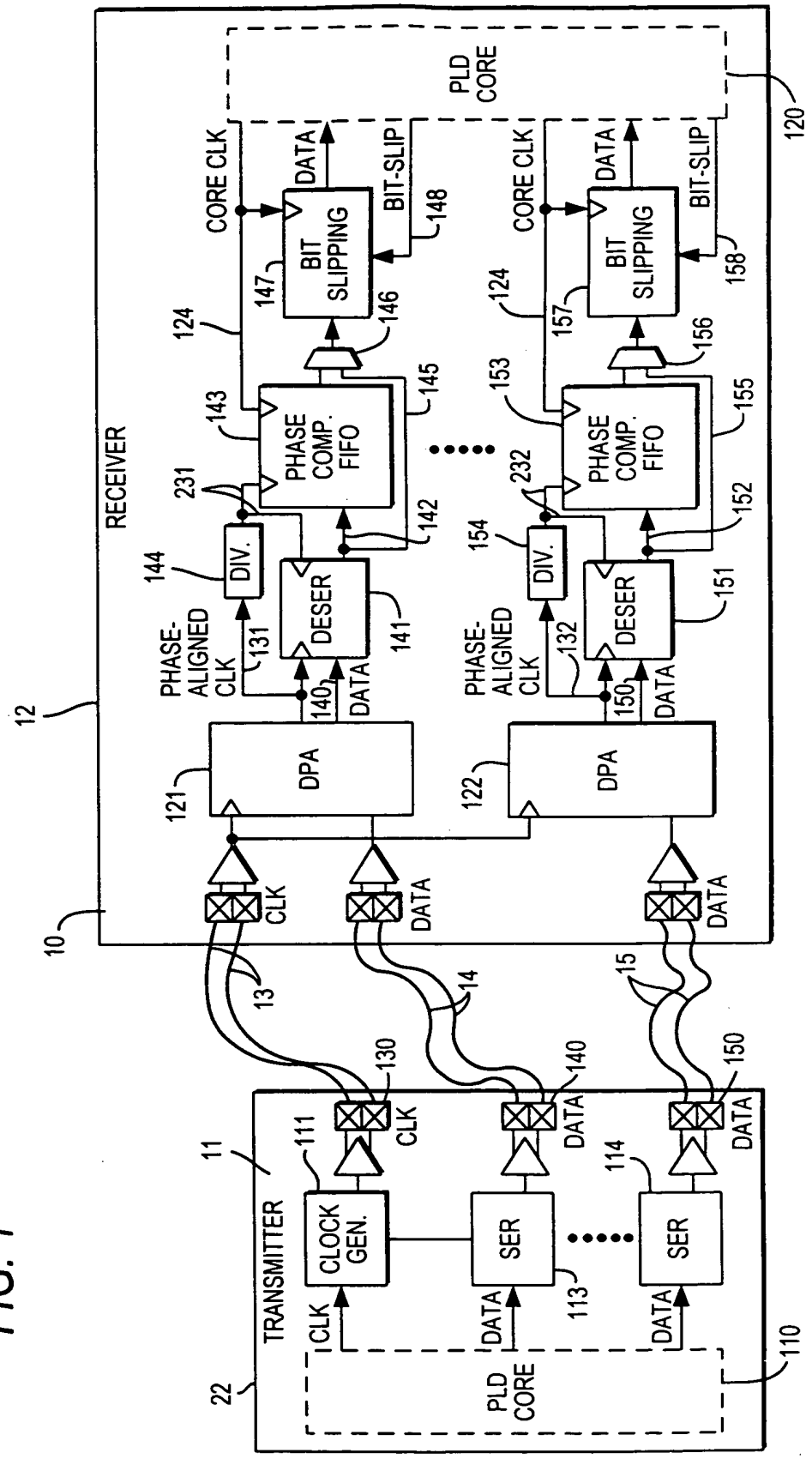
RECEIVER
TRANSMITTER
PLD CORE
CORE CLK
DATA
BIT-SLIP
BIT SLIPPING
PHASE COMP. FIFO
DIV.
DESER
PHASE-ALIGNED CLK
DPA
CLK
CLOCK GEN.
SER
10
11
12
13
14
15
22
110
111
113
114
120
121
122
124
130
131
132
140
141
142
143
144
145
146
147
148
150
151
152
153
154
155
156
157
158
231
232

FIG. 1

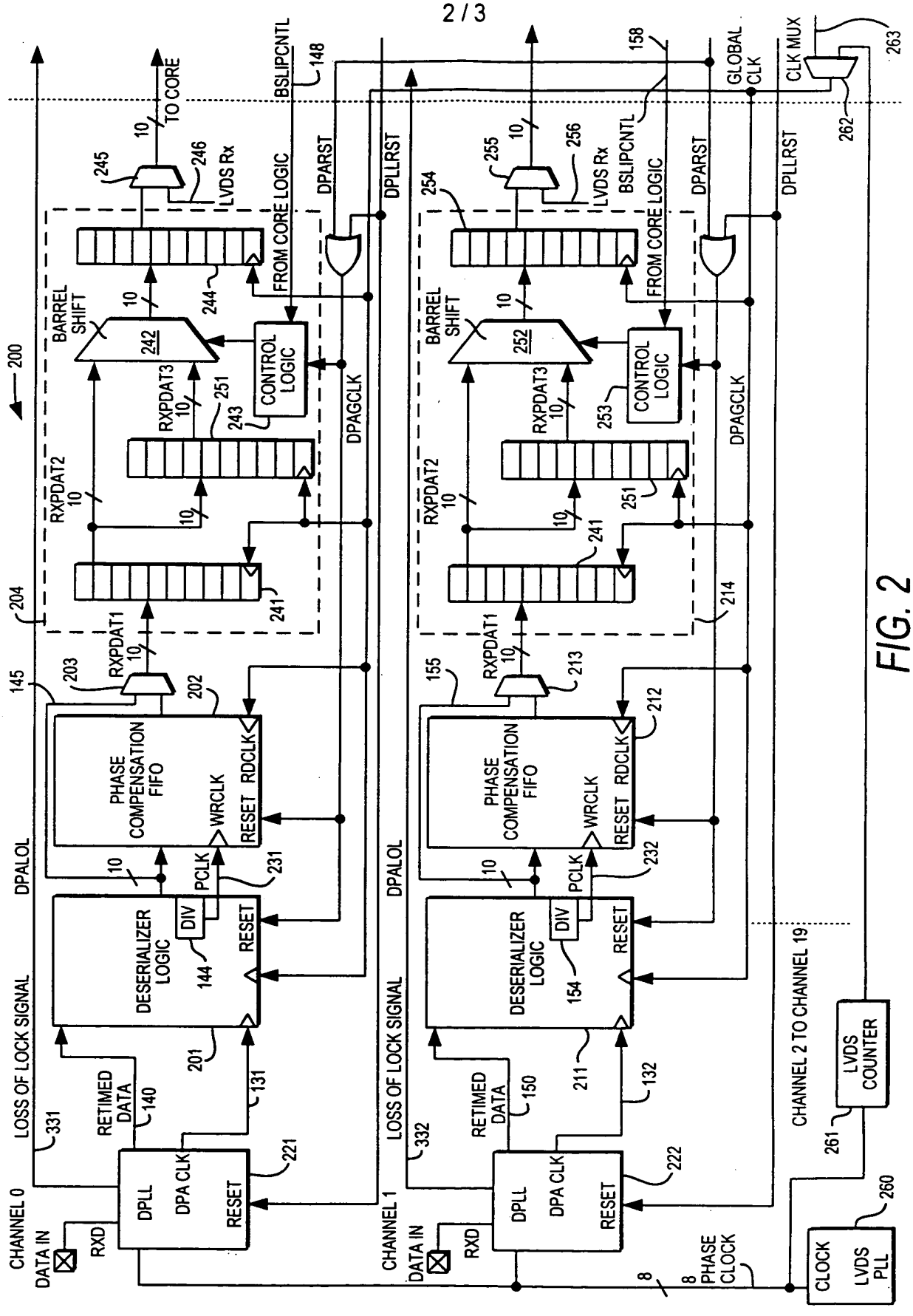
200
CHANNEL 0
DATA IN
RXD
DPLL
DPA CLK
RESET
LOSS OF LOCK SIGNAL
RETIMED DATA
140
331
221
131
201
DESERIALIZER LOGIC
DIV
144
RESET
PCLK
231
DPALOL
PHASE COMPENSATION FIFO
WRCLK
RDCLK
RESET
145
203
202
RXPDAT1
10
204
RXPDAT2
241
243
RXPDAT3
251
242
BARREL SHIFT
CONTROL LOGIC
FROM CORE LOGIC
244
245
246
LVDS Rx
TO CORE
DPAGCLK
DPARST
DPLLRST
BSLIPCNTL
148
CHANNEL 1
254
255
256
158
GLOBAL CLK
CLK MUX
263
262
CHANNEL 2 TO CHANNEL 19
LVDS COUNTER
261
CLOCK
LVDS PLL
260
PHASE CLOCK
8
214
212
213
155
211
132
150
154
222
332
252
253
241

FIG. 2

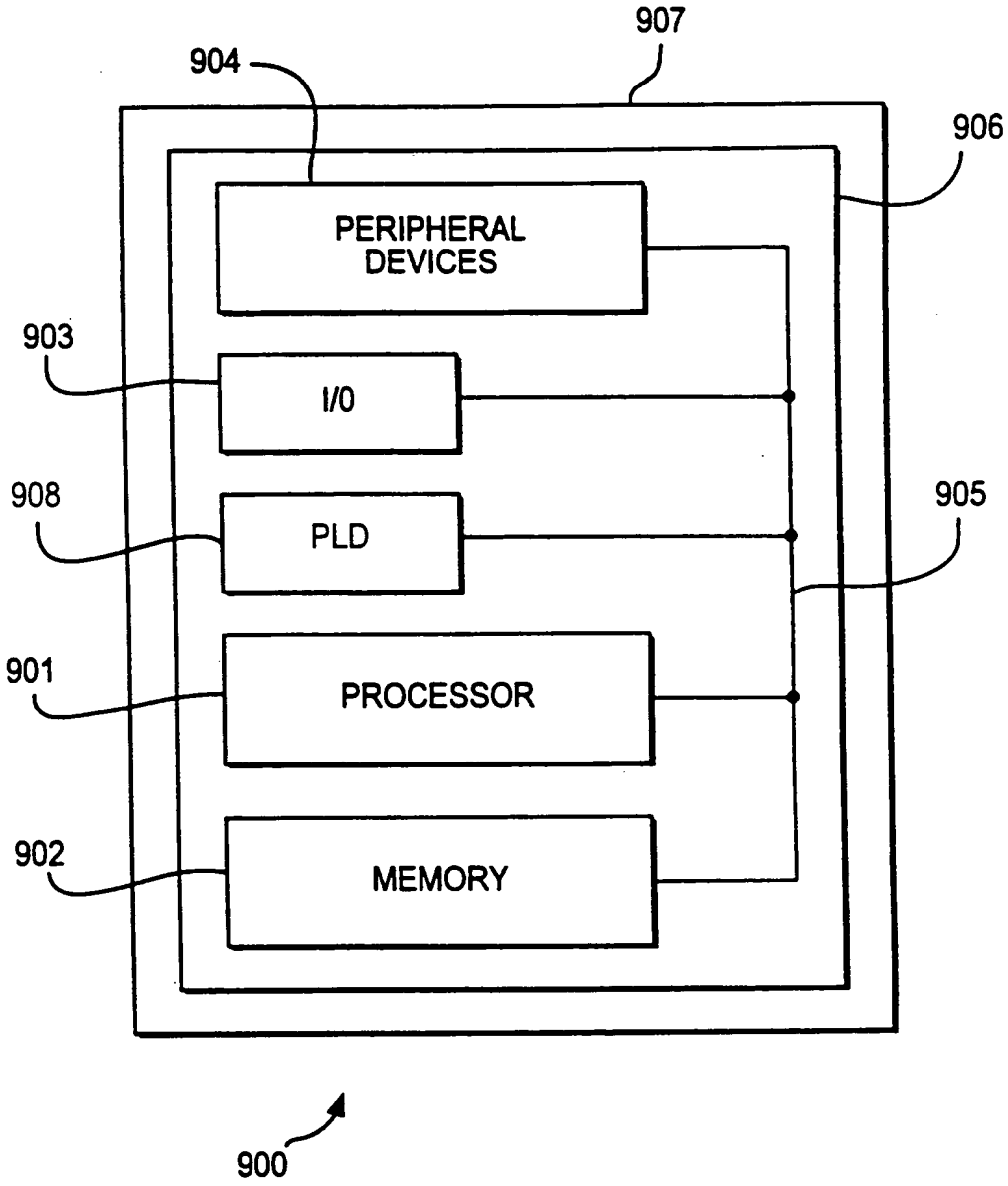
907
904
906
PERIPHERAL DEVICES
903
I/0
908
PLD
905
901
PROCESSOR
902
MEMORY
900

FIG. 3